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Clock control circuit and clock control method
US Pat. 6380774 - Filed Mar 23, 2001 - NEC Corporation
15 or counter 170 and decoders control signal connected to a control ... In other
words, when the interpolator is used, jitter per Upon receiving an output ...

Delay locked loop circuitry for clock delay adjustment
US Pat. 6539072 - Filed Mar 13, 2000 - Rambus, Inc.
Types of digital filters that can be employed to reduce loop jitter include a
... Loop 500 comprises a selection circuitry 510, phase interpolator 560, ...

Delay circuit and semiconductor integrated circuit having same
US Pat. 6369627 - Filed Jun 27, 2000 - Fujitsu Limited
As a result, the occurrence of jitter in the internal clock signal CLKI can be
prevented. The delay circuit 202 is provided with one interpolator 200 ...

Method for minimizing jitter using matched, controlled-delay elements slaved ...
US Pat. 6774686 - Filed Sep 28, 2001 - Intel Corporation
More particularly, the invention relates to the minimizing of jitter in a ...
The interpolator 270 also receives a control signal transmitted from the DLL ...

Timing interpolator
US Pat. 5206889 - Filed Jan 17, 1992 - Hewlett-Packard Company
The emitter degeneration in the control voltage differ- By making the delay of
... the control voltage in producing output phase jitter as with its input. ...

Delay-locked loop circuitry for clock delay adjustment
US Pat. 6125157 - Filed Feb 6, 1997 - Rambus, Inc.
The circuitry of claim 11, wherein the control circuit includes a digital storage
... phase interpolator. 13. The circuitry of claim 12, wherein the state ...

Phase locked loop for reducing electromagnetic interference
US Pat. 6703902 - Filed Sep 24, 2002 - Samsung Electronics Co. Ltd.
Accordingly, the jitter of the PLL can be reduced. That is, the phase interpolator
1115 divides the phase difference between two sequential clock signals ...

Method of an apparatus for correctly transmitting signals at high speed ...
US Pat. 6400616 - Filed Oct 27, 2000 - Fujitsu Limited
Since a phase interpolator of high frequency or a variable delay circuit of short
delay time causes little jitter, the timing signal generator circuit of ...

Time interval analyzer having interpolator with constant current capacitor ...

US Pat. 6091671 - Filed Jul 14, 1999 - Guide Technology, Inc.
Jitter typically refers to small, high frequency waveform variations caused by
mechanical vibrations, supply voltage fluctuations, control-system ...

Digital variable-delay circuit having voltage-mixing interpolator and ...
US Pat. 6348826 - Filed Jun 28, 2000 - Intel Corporation
10 In 242, the interpolator circuit's logic circuit (eg logic 2s circuit 101, FIG.
5) is controlled in response to a plurality of control codes, ...

Timing signal generating circuit, semiconductor integrated circuit device ...
US Pat. 6247138 - Filed Jun 8, 1998 - Fujitsu Limited
The delay units used for the phase interpolator operates with the control
signal (CS) from the master circuit (136 or 236) in the fine delay control block ...

Signal transmission system having a timing adjustment circuit
US Pat. 6484268 - Filed Feb 28, 2001 - Fujitsu Limited
That is, even when jitter is contained in the input reference clock CKr, ...
302 is provided with a fine delay control block using a phase interpolator 236, ...

Clock control circuit
US Pat. 6583655 - Filed May 16, 2002 - NEC Electronics Corporation
1 2 CLOCK CONTROL CIRCUIT In order to provide a clock control circuit that reduces
... 15 interpolator as a multiphase clock generating circuit 210 are 10 ...

Variable delay element
US Pat. 6133773 - Filed Oct 10, 1997 - Rambus Inc
Therefore, a linear phase interpolation transfer function is desired so that the
phase interpolator does not become more susceptible to jitter at certain ...

Timing signal generator for correctly transmitting a signal at high speed ...
US Pat. 6707727 - Filed Apr 22, 2002 - Fujitsu Limited
Since a phase interpolator of high frequency or a variable delay circuit of short
delay time causes little jitter, the timing signal generator circuit of ...

Method of and apparatus for correctly transmitting signals at high speed ...
US Pat. 6166971 - Filed Jun 1, 1999 - Fujitsu Limited
15 The output signal CKs of the phase interpolator 3012 is supplied to the
frequency divider .... According to a phase control code, the phase interpolator ...

[APPLICATION] Clock control circuit and clock control method
US Pat. App 9/815,846 - Filed Mar 23, 2001
In other words, when the interpolator is used, jitter per clock obtained by ...
15 to 20, a clock control circuit according to the present invention ...

Phase controlled oscillator
US Pat. 6617936 - Filed Jun 22, 2001 - Velio Communications, Inc.
This filters out more input clock jitter but at the expense of not rejecting ...
Aphase interpolator using an injection locked oscillator is shown in FIG. ...

Delay locked loop circuitry for clock delay adjustment
US Pat. 7039147 - Filed Feb 14, 2003 - Rambus Inc.
Loop 500 comprises a selection circuitry 510, phase interpolator 560, ...

Counter Control 240 and DAC 250 as in FIG. 4 to additionally reduce loop jitter. ...

Digital signal processing system in modem
US Pat. 5077755 - Filed Apr 23, 1990 - Fujitsu Limited
10 is a detail block diagram of an interpolator very high, shown in FIG. 8; Phase
jitter also occurs at double or three times of the FIG. ...

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Clock control circuit and clock control method
US Pat. 6380774 - Filed Mar 23, 2001 - NEC Corporation
Two mutually adjacent signals (of even and odd phases) selected by the switch
20A enter an interpolator (a phase interpolator) 30A, which delivers an output ...

Delay locked loop circuitry for clock delay adjustment
US Pat. 6539072 - Filed Mar 13, 2000 - Rambus, Inc.
Types of digital filters that can be employed to reduce loop jitter include a
... Loop 500 comprises a selection circuitry 510, phase interpolator 560, ...

Phase locked loop for reducing electromagnetic interference
US Pat. 6703902 - Filed Sep 24, 2002 - Samsung Electronics Co. Ltd.
Accordingly, the jitter of the PLL can be reduced. That is, the phase interpolator
1115 divides the phase difference between two sequential clock signals ...

Method of and apparatus for correctly transmitting signals at high speed ...
US Pat. 6166971 - Filed Jun 1, 1999 - Fujitsu Limited
Namely, the signals SCl and SC2 control the delay (phase) of the first timing
signal CKs ... According to a phase control code, the phase interpolator ...

Variable delay element
US Pat. 6133773 - Filed Oct 10, 1997 - Rambus Inc
The phase interpolator circuit is a part of the clock recovery and alignment
circuitry. ... the control signals by considering any combination of frequency, ...

Delay circuit and semiconductor integrated circuit having same
US Pat. 6369627 - Filed Jun 27, 2000 - Fujitsu Limited
That is, 5 when the interpolator 196-4 has delayed a phase by 350° with respect
.... circuit 204 can control the composition of the internal clock signals ...

Method of an apparatus for correctly transmitting signals at high speed ...
US Pat. 6400616 - Filed Oct 27, 2000 - Fujitsu Limited
The output signal CKs of the phase interpolator 3012 is supplied to the frequency
... Namely, the signals SCl and SC2 control the delay (phase) of the first ...

Clock recovery using clock phase interpolator
US Pat. 7180352 - Filed Jun 28, 2001 - Intel Corporation
45 The control signals for clock phase interpolator 700 include select signals
... phases in one circuit stage, reducing both power consumption and jitter. ...

Delay-locked loop circuitry for clock delay adjustment

US Pat. 6125157 - Filed Feb 6, 1997 - Rambus, Inc.
The circuitry of claim 11, wherein the control circuit includes a digital ...
of adjacent phase vector signals from the set; a phase interpolator circuit ...

Clock control circuit
US Pat. 6583655 - Filed May 16, 2002 - NEC Electronics Corporation
Two mutually adjacent signals enter signal C/CB to the interpolator 130. ...
On the basis of the result of detecting a shown) and the phase of the output ...

N-way circular phase interpolator for generating a signal having arbitrary phase
US Pat. 6329859 - Filed Mar 23, 2000 - BitBlitz Communications, Inc.
The associated control logic table of a four-way circular phase interpolator is
shown in Table II below. As seen from Table II, four phase signals 9A, QB, ...

Timing signal generator for correctly transmitting a signal at high speed ...
US Pat. 6707727 - Filed Apr 22, 2002 - Fujitsu Limited
65 To transmit signals at high speed, jitter in the DLL and PLL circuits must be
... However, it is difficult to realize a phase interpolator that operates ...

Clock synchronization circuit and semiconductor device having the same
US Pat. 6385126 - Filed Jan 11, 2001 - Samsung Electronics Co., Ltd.
The phase interpolator 141 interpolates the phases of signals <P' and 'P' output
from the ... circuit is increased, so that jitter performance is degraded. ...

DLL calibrated switched current delay interpolator
US Pat. 6094082 - Filed May 18, 1998 - National Semiconductor Corporation
In contrast, the present approach uses the phase interpolator described to ...
corresponding first and second control signals, the first control signal ...

Source synchronous interface using variable digital data delay lines
US Pat. 6791360 - Filed Sep 11, 2002 - Sun Microsystems, Inc.
The zero degree phase jitter; local clock signal provides good transition ...
phase interpolator (340), code on the digital signals on signal paths (252) ...

Method for minimizing jitter using matched, controlled-delay elements slaved ...
US Pat. 6774686 - Filed Sep 28, 2001 - Intel Corporation
Interpolator 270 receives four different phase clock inputs ie, ... transmitted from
the DLL 200 and a signal from the interpolator control circuitry 240. ...

Delay locked loop circuitry for clock delay adjustment
US Pat. 7039147 - Filed Feb 14, 2003 - Rambus Inc.
Types of digital filters that can be employed to reduce loop jitter include a
... Loop 500 comprises a selection circuitry 510, phase interpolator 560, ...

Phase interpolator based clock recovering
US Pat. 7197101 - Filed Jan 2, 2002 - Intel Corporation
1 2 PHASE INTERPOLATOR BASED CLOCK signals from the VCO or from a ... of a phase
interpolator nals, noise in the data signal, such as transmitter jitter, ...

Method and apparatus for correcting for clock and carrier frequency offset ...
US Pat. 5206886 - Filed Apr 16, 1990 - Telebit Corporation
FIG. shows a typical phase/frequency plot for These feedback algorithms afe ...

(of signal and jitter), pling time of the received signal or an interpolator ...

[APPLICATION] Voltage controller for a highly linear phase interpolator
US Pat. App 10/039,374 - Filed Jan 2, 2002
Further, channel jitter can result from phase dispersion, ... controller to
generate interrelated control signals for a highly linear phase interpolator. ...

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